Automating High and Low Frequency C-V Measurements and Interface Trap Density (DIT) Calculations of MOS Capacitors using the 4200A-SCS Parameter Analyzer

APPLICATION NOTE

KEITHLEY
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Introduction

Capacitance-voltage (C-V) measurements are commonly used in studying gate-oxide quality. These measurements are made on a two-terminal device called a MOS capacitor (MOS cap), which is basically a MOSFET without a source and drain. C-V test data on MOS capacitors offers a wealth of device and process information, including bulk and interface charges. Many MOS capacitor parameters, such as oxide thickness, flatband voltage, threshold voltage, etc., can be extracted from the high frequency C-V data. However, one parameter, the interface trap density (DIT), is typically derived from both the high and low frequency C-V measurements. Typically performing both types of C-V sweeps requires two different measuring instruments with two different types of cable sets requiring the user to physically change prober connections between measurements. However, using the Keithley 4200A-SCS Parameter Analyzer with the appropriate modules enables the user to make both high and low frequency measurements without recabling.

When configured with two source measure units (SMUs) with preamps and a capacitance voltage unit (CVU), the 4200A-SCS Parameter Analyzer can perform both high and low frequency C-V measurements. The 4200A-CVIV Multi-Switch enables the user to automatically switch between high and low frequency measurements without having to change cables or lift the probe tips. The Clarius software that is included with the 4200A-SCS has an extensive library with built-in tests for making C-V measurements on MOS capacitors including a project that combines both high and low frequency measurements. This project extracts many common C-V parameters including the interface trap density (DIT).

This application note discusses how to use the 4200A-SCS Parameter Analyzer to measure and to automatically switch between high and low frequency C-V measurements on MOS capacitors. Basic information on MOS capacitors and common parameter extractions is also discussed.

The MOS Capacitor

Figure 1 illustrates the construction of a MOS capacitor. Essentially, a MOS capacitor is just an oxide placed between a semiconductor and a metal gate. The semiconductor and metal gate are the two plates of the capacitor. The oxide functions as the dielectric. The area of the metal gate defines the area of the capacitor.

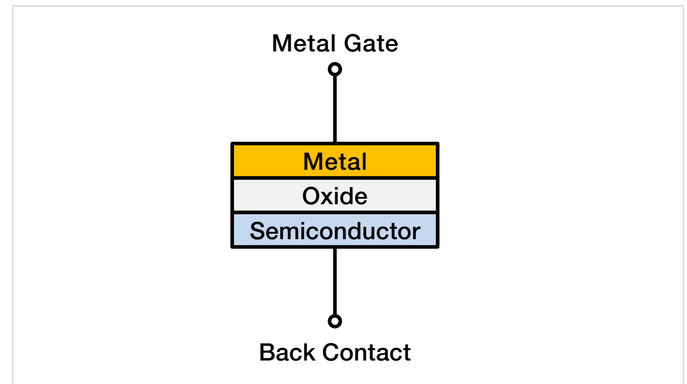

Figure 1. MOS capacitor.

An important property of the MOS capacitor is that its capacitance changes with an applied DC voltage. As a result, the modes of operation of the MOS capacitor change as a function of the applied voltage. Further information on MOS capacitors and making C-V measurements on them can be found in the Keithley application note, *"C-V Characterization of MOS Capacitors Using the 4200A-SCS Parameter Analyzer".*

Hardware Requirements for Automating High and Low Frequency C-V Measurements

To automate between high and low frequency C-V measurements, the 4200A-SCS Parameter Analyzer must be configured with at least the options listed in **Table 1**.

Qty	Module	Description	Purpose
2	4200-SMU, 4201-SMU, 4210-SMU, or 4211-SMU	Source Measure Units (SMU)	Measures very low frequency (VLF) C-V
2	4200-PA	Preamps for SMUs	Measuring high impedance requires measuring very small current
1	4215-CVU or 4210-CVU	Capacitance Voltage Unit (CVU)	Measures high frequency C-V
1	4200A-CVIV	Multi-Switch	Enables automatic switching between low frequency and high frequency measurements

Table 1. Required modules.

Additional cabling is necessary to connect between the output of the 4200A-CVIV and the probe station. We recommend using the 4200-TRX-.75 Triax Cables on the output of the CVIV. These shielded cables are used to ensure that both very low current and high frequency AC measurements can be made with high accuracy.

Installing and Configuring the 4200A-CVIV

Installing and configuring the 4200A-CVIV consists of making connections to its input terminals and output terminals and updating the 4200A-CVIV configuration in the KCON application.

Input and output connections

The CVU and the preamps of the SMUs are connected to the input terminals of the 4200A-CVIV as shown in **Figure 2**. SMU1 and SMU2 are connected to CH1 and CH2. Either two additional SMUs or channel blocks (included with the CVIV) are connected to CH3 and CH4 inputs.

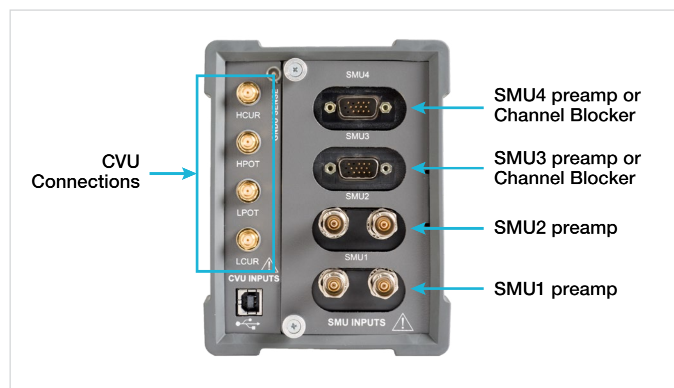

Figure 2. Input connections on the 4200A-CVIV.

The output terminals of the CVIV are connected to the prober. CH1 is connected to the gate of the MOS capacitor and is used to measure the capacitance. CH2 is connected to the substrate, or chuck, and is used to apply the DC voltage. More information on making proper connections to make optimal C-V measurements can be found in the Keithley application notes listed in Appendix B.

Configuring the Setup in KCON

After the SMUs and CVU are connected to the CVIV, make sure the CVIV is connected to the 4200A-SCS with the supplied USB cable. Close the Clarius application and open the KCON application on the desktop. At the top of the screen, select Update. Once the unit is done updating, select Save. Open Clarius to begin configuring the Clarius software.

Selecting and Configuring the *moscap-cv-dit-cviv* Project for C-V Measurements

The built-in library of the Clarius application includes several tests and projects that perform high and low frequency measurements on MOS capacitors. With the Clarius V1.9 release, a new project, *moscap-cv-dit-cviv*, has been added to the Projects Library. This project switches between high and low frequency C-V sweeps and includes the calculation of the interface trap density (DIT). This project can be found in the library in the Select view search bar by entering DIT. By selecting and then creating the project, the *moscap-cv-dit-cviv* project will appear in the project tree as shown in **Figure 3**. The following sections will describe the tests in the project tree.

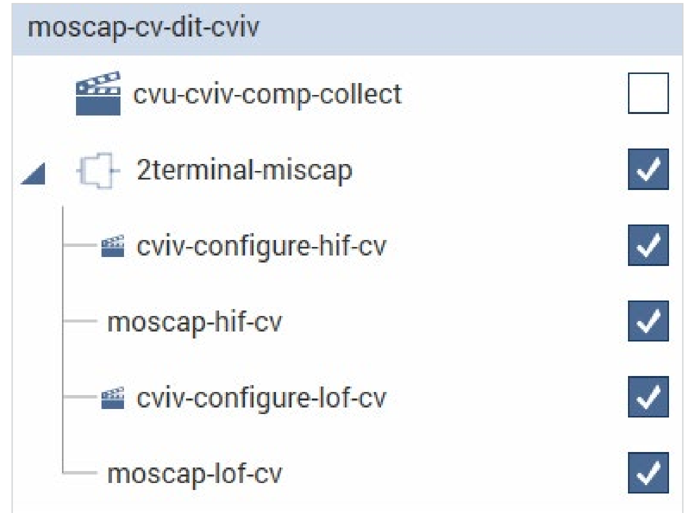

Figure 3. Project tree of *moscap-cv-dit-cviv* project.

Acquiring CVU Compensation Data

The first item listed in the project tree is the *cvu-cviv-comp-collect* Action for acquiring compensation data. CVU Connection Compensation is used to correct for offset and gain errors caused by the connections between the CVU and the device under test (DUT). In this case, the connections are from the CVU through CH1 and CH2 of the CVIV and to the cabling to the probe and chuck. This Action is Run with the probes up. A screen capture of the Configure view of the *cvu-cviv-comp-collect* Action is shown in **Figure 4**.

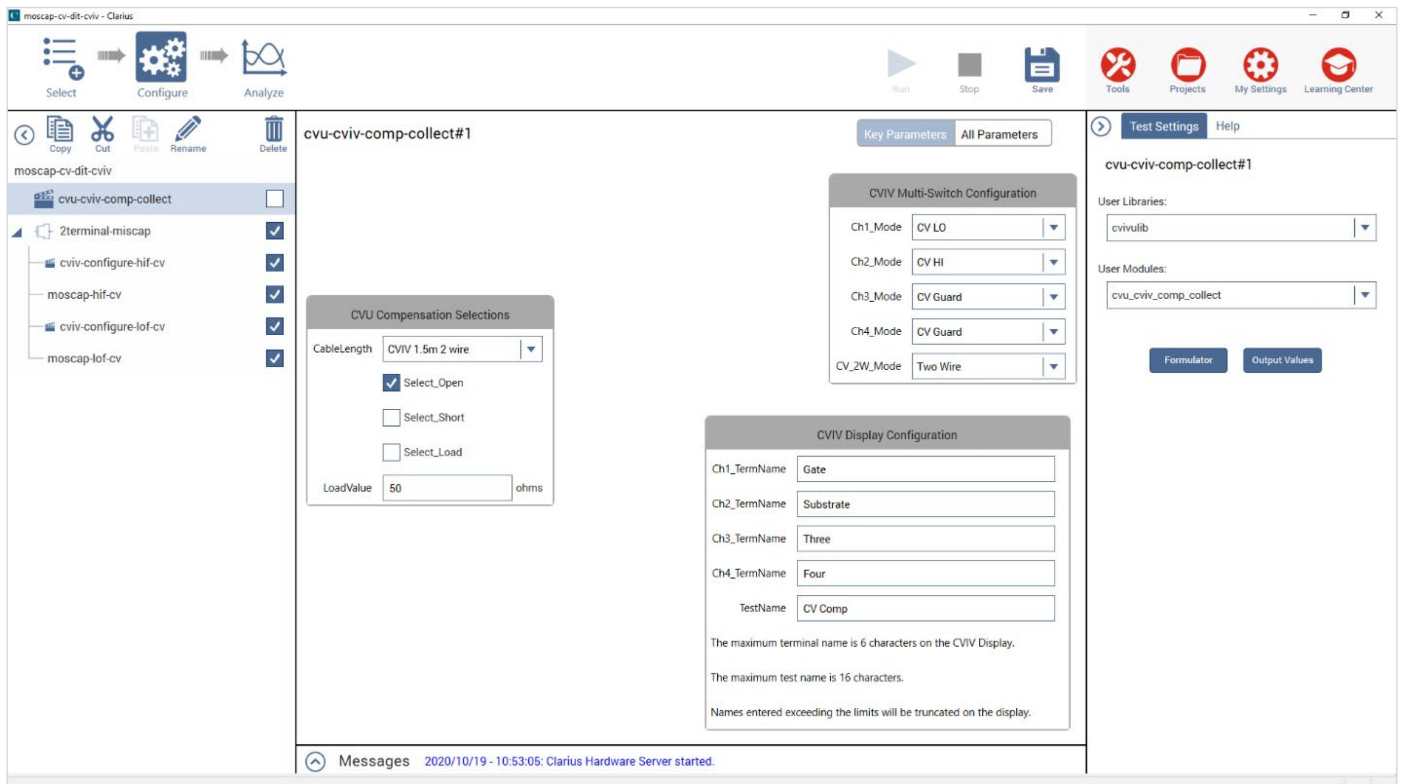

Figure 4. Configure view of the *cvu-cviv-comp-collect* Action for acquiring compensation data.

Switching Between the CVU and SMUs

The *cviv-configure-hif-cv* and *cviv-configure lof-cv* actions are used to automatically switch the outputs of CH1 and CH2 of the CVIV between the CVU and the two SMUs. This prevents unnecessary disturbances of the cabling and connections to the device during the test.

The CVU connections through the CVIV are shown in **Figure 5**. In this case, CVH terminal is connected through CH 1 to the substrate of the MOS cap and forces the DC bias voltage. The CVL terminal is connected through CH 2 to the gate of the MOS cap and measures the ac current. Even though CH 3 and CH4 are unused, these channels are configured for CV Guard to minimize noise from unwanted pathways. A screen capture of the *cvu-configure-hif-cv* Action is shown in **Figure 6**.

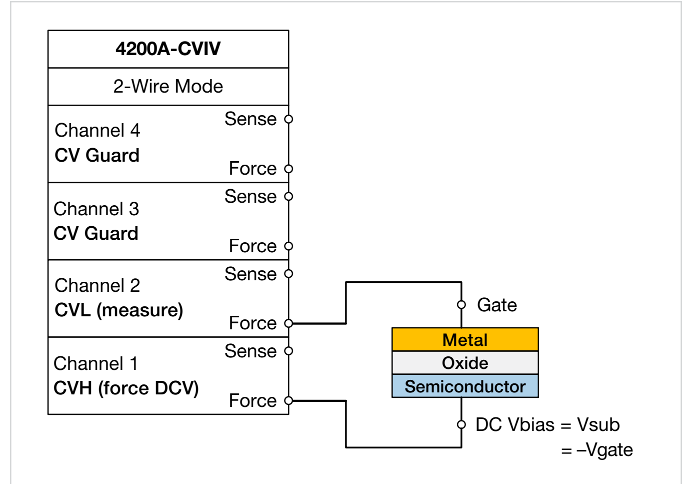

Figure 5. CVU connections through the 4200A-CVIV to the MOS capacitor.

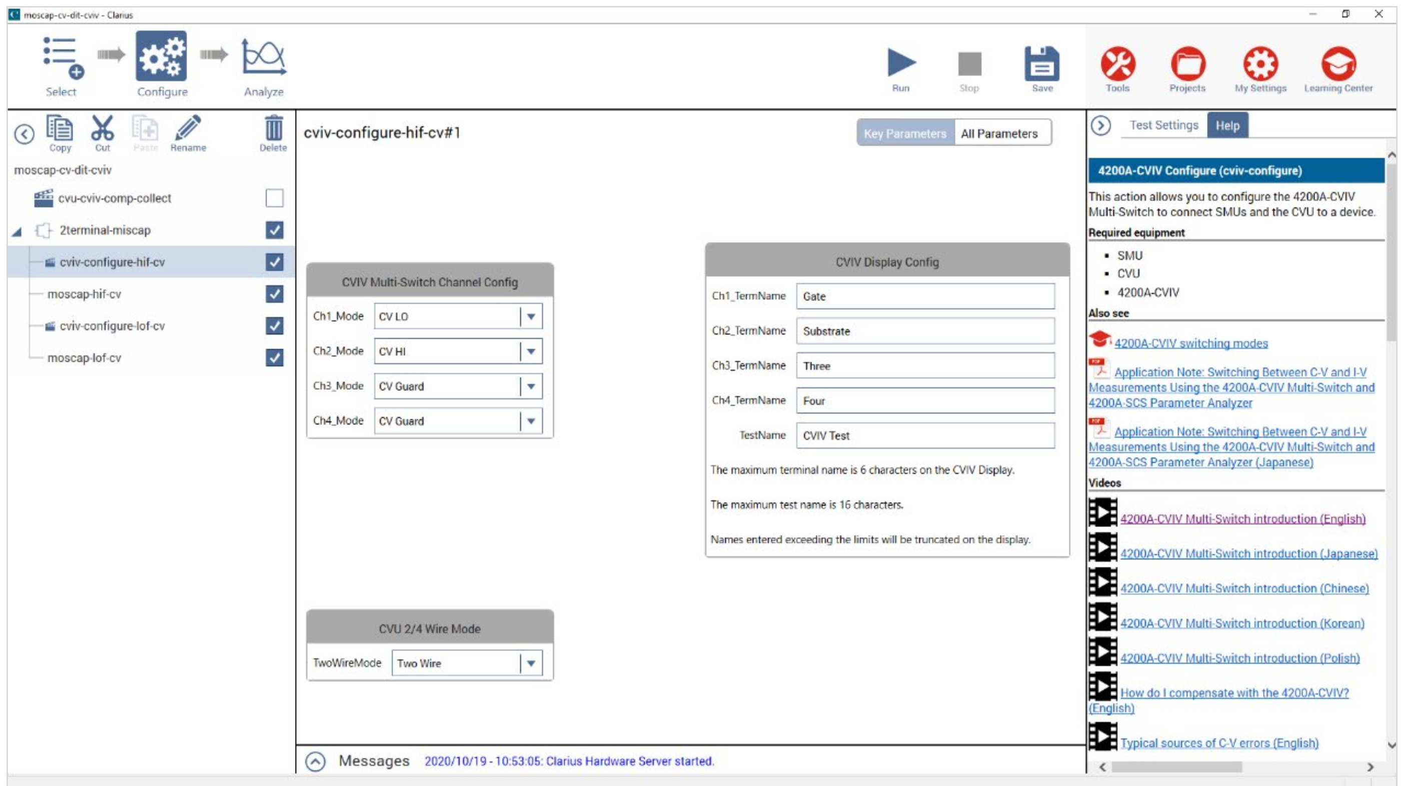

Figure 6. Configuration view of *cviv-configure-hif-cv action*.

Figure 7 shows the SMU connections through the CVIV for the low frequency C-V measurements. SMU1 is connected through CH1 to the substrate and SMU2 is connected through CH2 to the gate. Just like for the high frequency CVU measurements, the DC bias is applied to the substrate so that the gate voltage = (-1)*Vsubstrate.

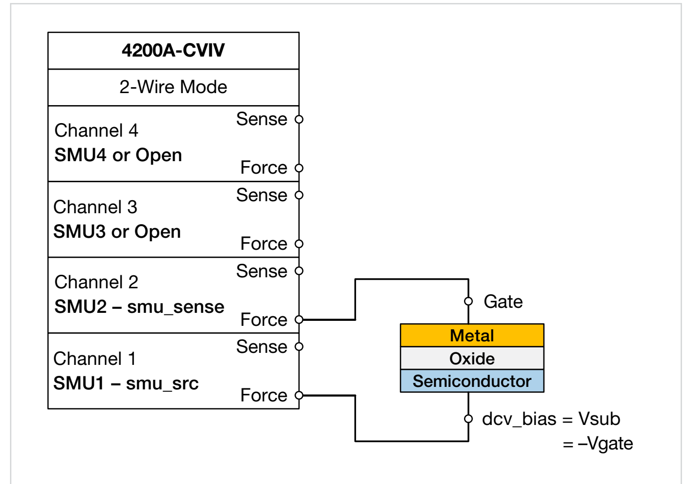

Figure 7. SMU connections through the 4200A-CVIV for MOS capacitor measurements.

High Frequency Measurements Using the CVU

The 4215-CVU or 4210-CVU Capacitance Voltage Unit can measure capacitance with a range of test frequencies from 1 kHz to 10 MHz. The *moscap-hif-cv* test in the project is configured for making a C-V sweep with the CVU. The test parameters, such as the test frequency, DC bias, and timing settings, can be adjusted in the Configure view of the test, which is shown in **Figure 8**. To enable the CVU offset compensation, check the appropriate Compensation boxes in the Terminal Settings window.

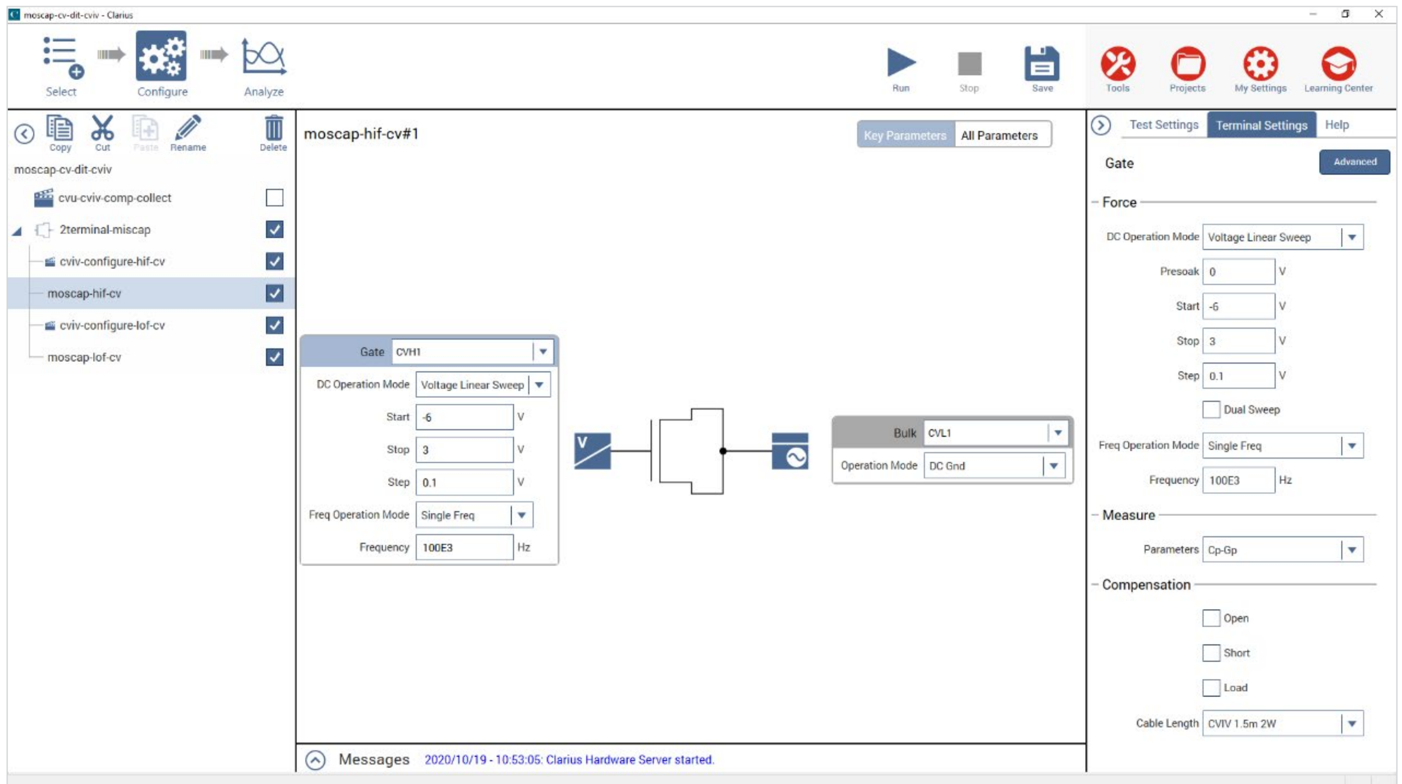

Figure 8. Configure view of the *moscap-hif-cv* test.

This test has calculations in the Formulator for deriving and adjusting for the series resistance. The formulas in this test are listed in Appendix A. Some of the constants in the Formulator including the gate area and temperature will need to be adjusted prior to executing the test.

Once the test is Run, the graph is automatically generated. **Figure 9** shows the results of measuring an n-type MOS capacitor using the test.

Keithley application notes for making optimal high frequency C-V measurements on MOS capacitors are listed in Appendix B.

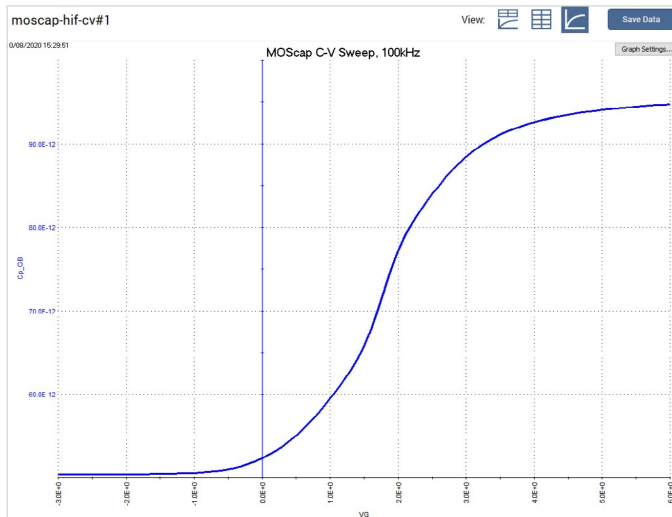

Figure 9. C-V sweep of MOS capacitor using the 4215-CVU.

Low Frequency Measurements Using Two SMUs

The 4200A-SCS makes low frequency C-V measurements using the very low frequency (VLF) C-V technique, which uses the low current measurement capability of the SMUs to perform C-V measurements at specified low frequencies in the range of 10 mHz to 10 Hz. The VLF C-V technique requires two SMUs with preamps.

Figure 10 is a simplified diagram of the SMU instrument configuration used to generate the low frequency impedance measurements. SMU1 outputs the DC bias with a superimposed AC signal and measures the voltage. SMU2 measures the resulting AC current while sourcing 0 V DC.

More detailed information on the VLF-CV technique can be found in the Keithley application note, *"Performing Very Low Frequency Capacitance-Voltage Measurements on High Impedance Devices Using the 4200A-SCS Parameter Analyzer"*.

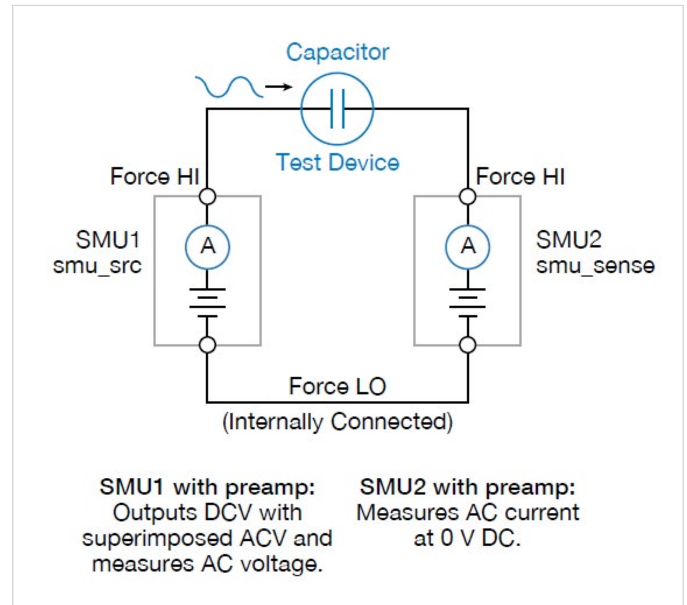

Figure 10. VLF C-V measurement setup for a MOS capacitor on wafer.

The *moscap-lof-cv* test in the project tree is used for making a very low frequency C-V sweep on the MOS capacitor. Test parameters can be adjusted in the Configure view, shown in **Figure 11**.

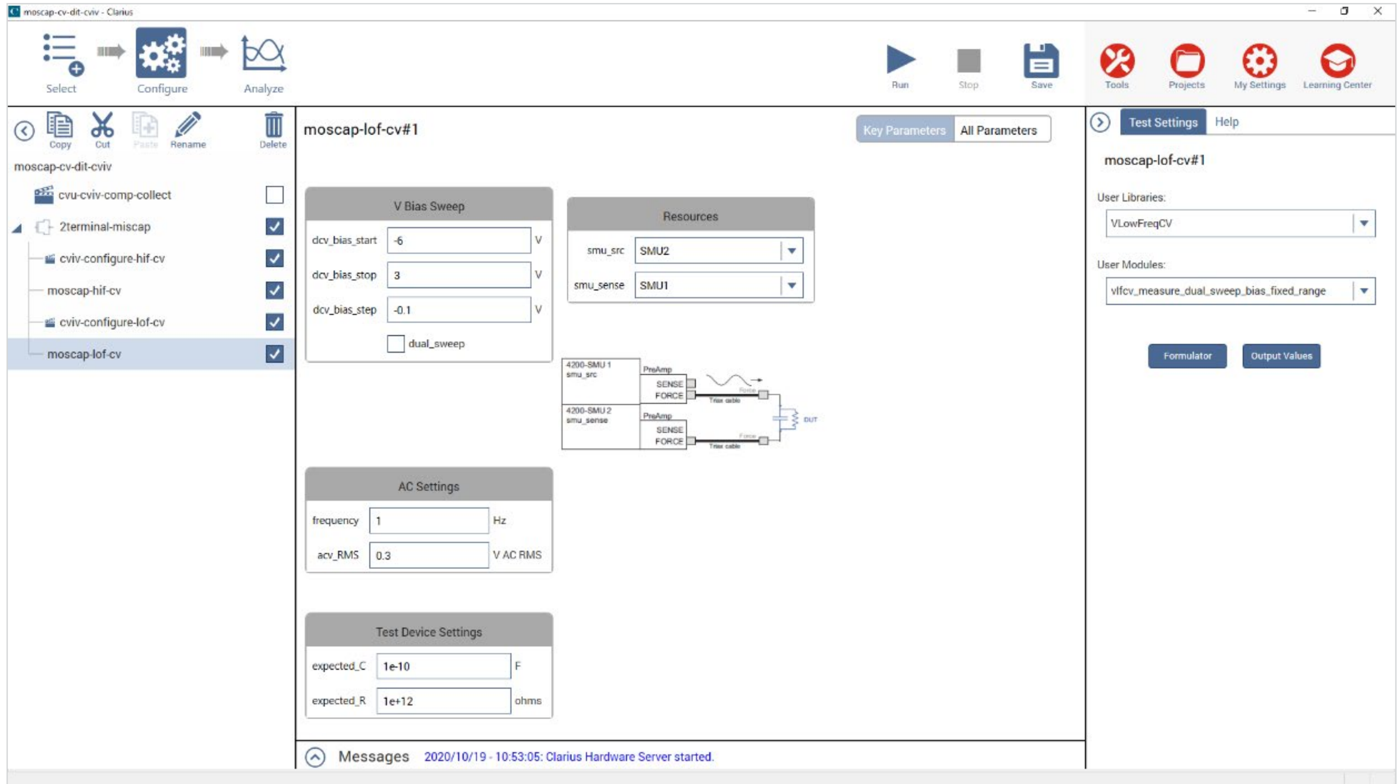

Figure 11. Configure view of the *moscap-lof-cv* test.

Once the test is Run, the graph is automatically generated as shown in **Figure 12**.

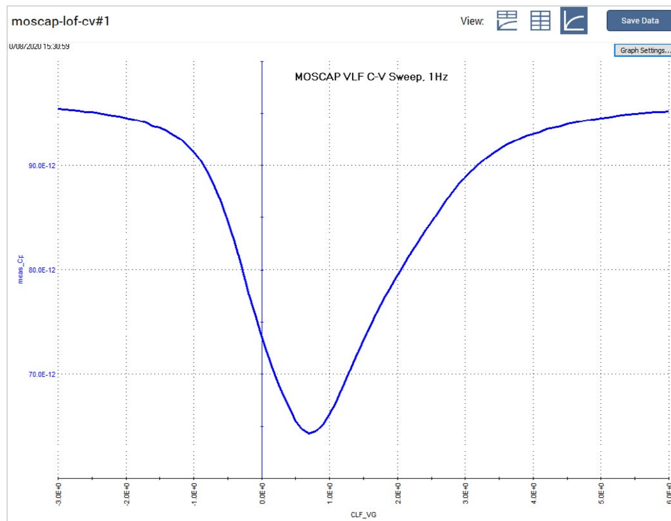

Figure 12. Very low frequency (VLF) C-V sweep of MOS capacitor.

Executing the *moscap-cv-dit-cviv* project and parameter extractions

When the *moscap-cv-dit-cviv* project is selected and is executed from the top of the project tree, the actions and tests will sequentially execute in their order in the project tree. The high and low frequency C-V measurements are sent to the project level Analyze Sheet and Graph and are plotted as shown in **Figure 13**.

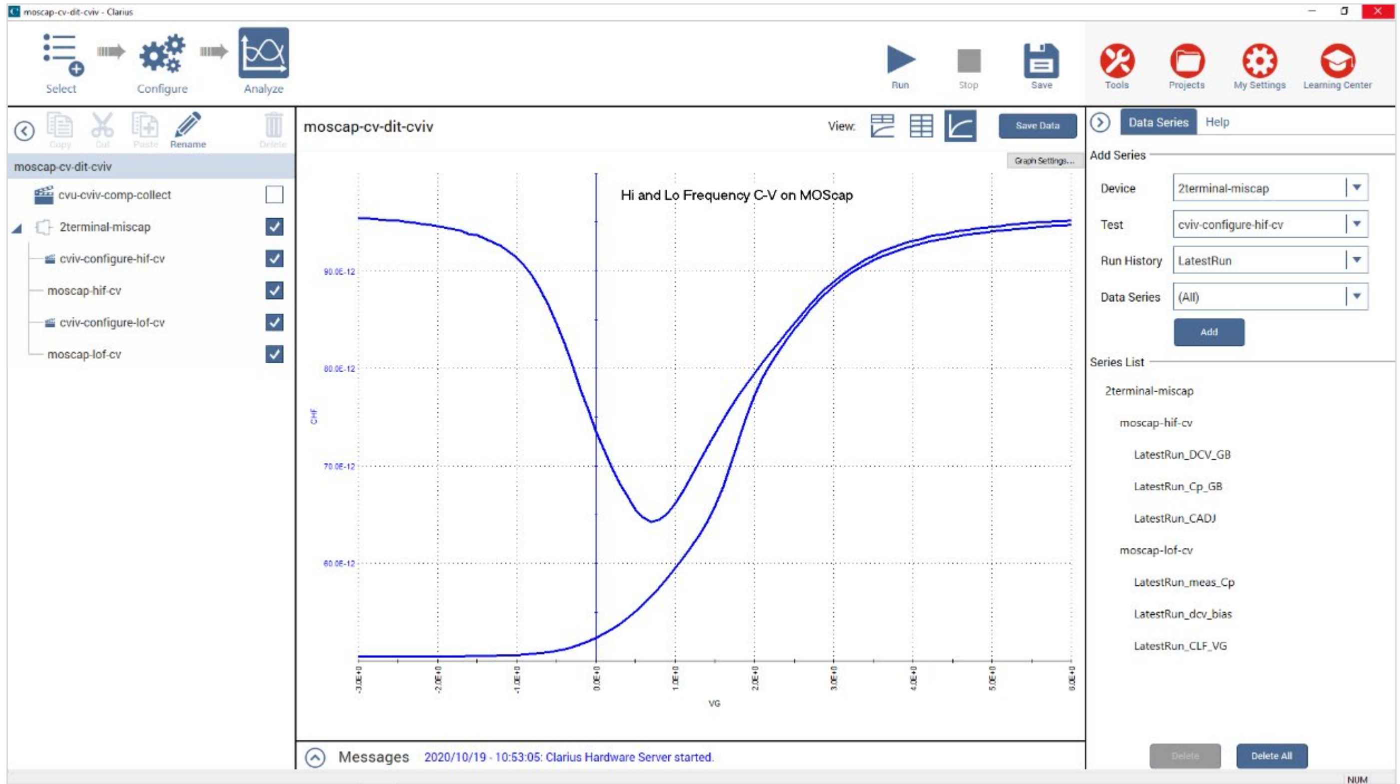

Figure 13. HI and LO Frequency C-V curves plotted in the project level Analyze view.

The C-V measurements are combined in equations in the formulator to calculate many MOS capacitor parameters including the flatband capacitance, flatband voltage, oxide capacitance, and the interface trap density as shown in **Figure 14**. Appendix A lists all the calculated parameters found at the project level Analyze view as well as in the *moscap-hif-cv* test in the project tree.

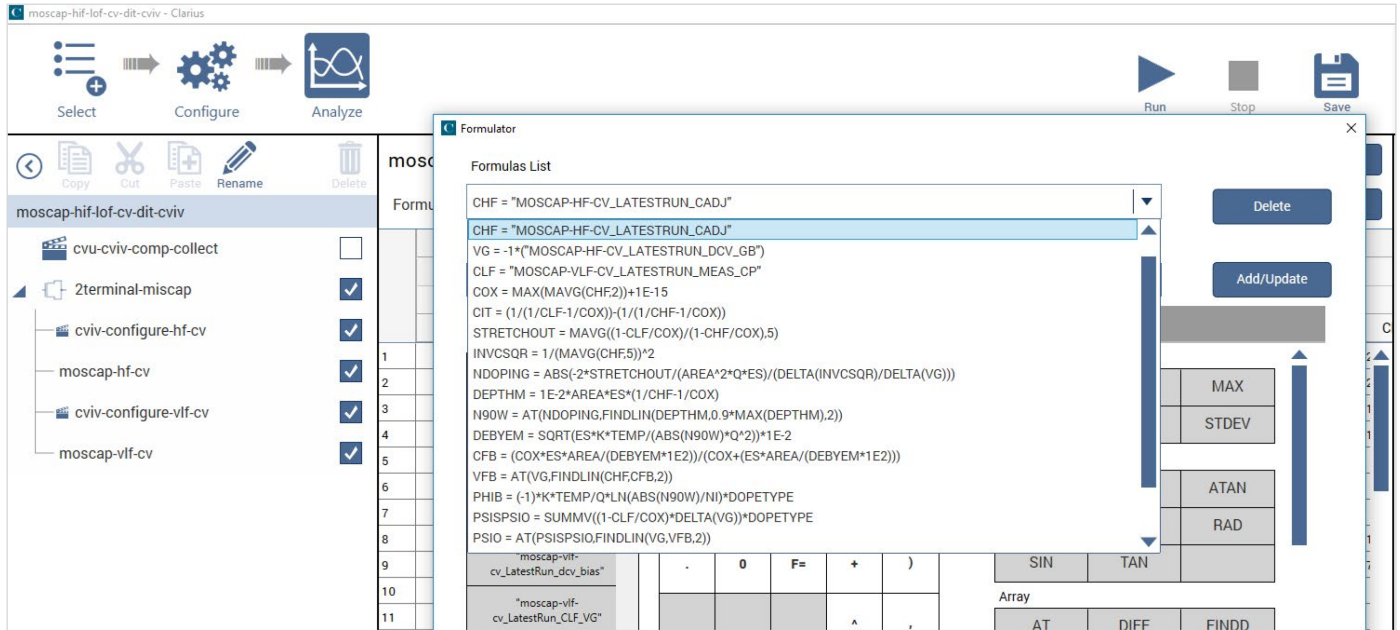

Figure 14. Project level Formulas List.

Interface Trap Density (DIT)

From the calculated parameters in the project level, the interface trap density (DIT) is derived and can be plotted. Interface traps are defects or impurities resulting from processing or device damage. These traps are located at the semiconductor interface and can be charged or discharged and affect the device capacitance. Because traps may respond slowly to changes in gate voltage, they affect the device capacitance at high frequencies but not low frequencies. DIT can be plotted against the interface trap energy (eV) with respect to mid band gap as shown in **Figure 15**.

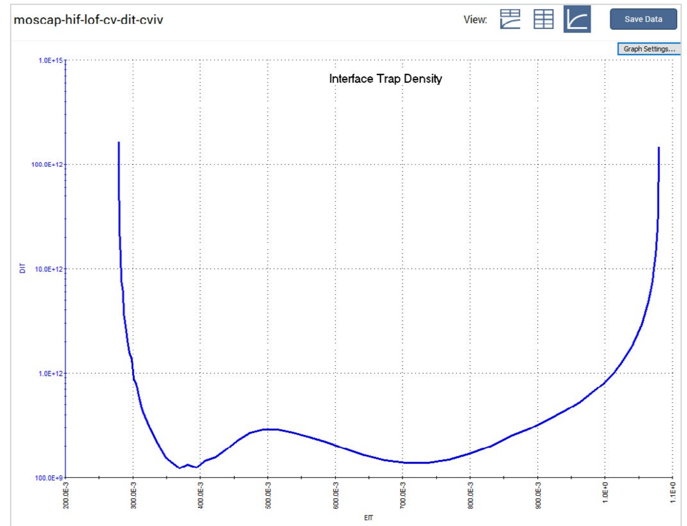

Figure 15. Interface trap density graphed in project level Analyze View Graph.

Conclusion

High and low frequency C-V measurements can be automated using two SMUs with preamps, a CVU, the 4200A-CVIV Multi-Switch, and the Clarius software. From the C-V data, many important device parameters are derived including the interface trap density. Techniques for making optimal high and low frequency C-V measurements are found in the applications notes listed in Appendix B.

Appendix A: Project Formulas and Constants

Project Level Calculations in the Formulator

Formula	Description
CHF	Adjusted high frequency capacitance from the latest Run of the moscap-hf-cv test: CHF= “MOSCAP-HF-CV_LATESTRUN_CADJ”
VG	Since the DC voltage is applied to the substrate, VG=-Vsubstrate, and is updated from the latest Run of the moscap-hf-cv test: VG= -1*(“MOSCAP-HF-CV_LATESTRUN_DCV_GB”
CLF	Low frequency capacitance from the latest Run of the moscap-vlf-cv test: CLF=”MOSCAP-VLF-CV_LATESTRUN_MEAS_CP”
COX	Oxide capacitance: COX = MAX(MAVG(CHAF,2))+1E-15
CIT	Interface trap capacitance: CIT=(1/(1/CLF-1/COX)-1/(1/CHF-1/COX))
STRETCHOUT	Stretch out factor due to interfacial states: STRETCHOUT = MAVG((1-CLF/COX)/(1-CHF/COX),5)INVCSQR = 1/(MAVG(CHF,5))^2
INVCSQR	Inversed square of high frequency capacitance: INVCSQR = 1/(MAVG(CHF,5))^2
NDOPING	Doping density: NDOPING = ABS(-2*STRETCHOUT/(AREA^2*Q*ES)/(DELTA(INVCSQR)/DELTA(VG)))
DEPTH	Depletion depth (in meters): DEPTHM = 1E-2*AREA*ES*(1/CHF-1/COX)
N90W	Doping density at 90% of maximum depletion depth: N90W = AT(NDOPING,FINDLIN(DEPTHM,0.9*MAX(DEPTHM),2))
DEBYEM	Debye length (in meters): DEBYEM = SQRT(ES*K*TEMP/(ABS(N90W)*Q^2))*1E-2
CFB	Flatband capacitance: CFB = (COX*ES*AREA/(DEBYEM*1E2))/(COX+(ES*AREA/(DEBYEM*1E2)))
VFB	Flatband voltage: VFB = AT(VGS,FINDLIN(CHF,CFB,2))
PHIB	Bulk Potential: PHIB = (-1)*K*TEMP/Q*LN(ABS(N90W)/NI)*DOPETYPE
PSISPSIO	PSIS-PSIO, which is surface potential: PSISPSIO = SUMMV((1-CLF/COX)*DELTA(VG))*DOPETYPE
PSIO	Offset in surface potential due to calculation method and flatband voltage: PSIO = AT(PSISPSIO,FINDLIN(VG,VFB,2))
PSIS	Silicon surface potential, ϕ_s. More precisely, this value represents band bending and is repeated to surface potential via the bulk potential. PSIS = PSISPSIO-PSIO
EIT	Interface trap energy (eV) with respect to mid band gap: EIT = PSIS+PHIB
DIT	Interfacial states density (cm^-2eV^-1): DIT = CIT/(AREA*Q)

Constants in Project level Sheet Formulator

Name	Default Value	Unit	Description
ES	1.04E-12	F/cm	Semiconductor permittivity
DOPETYPE	-1		1 = p-type -1 = n-type
TEMP	300	K	Test temperature
AREA	0.0025	cm^2	Gate area
NI	1.45E+10	cm^-3	Ni – intrinsic carrier concentration

Formulas for *moscap-hf-cv* test:

Formula	Description
VG	Gate voltage: VG = -DCV_GB
RS	Series Resistance calculated from capacitance in strong accumulation and conductance: RS = (AT(MAVG(GP_GB, 5)/((2*PI*F_GB)*MAVG(CP_GB, 5)), MAXPOS(MAVG(CP_GB, 5))))^2/((1+(AT(MAVG(GP_GB, 5)/((2*PI*F_GB)*MAVG(CP_GB, 5)), MAXPOS(MAVG(CP_GB, 5))))^2)*(AT(MAVG(GP_GB, 5),MAXPOS(MAVG(CP_GB, 5)))))
AR	Intermediate parameter for calculation of corrected capacitance: AR = GP_GB-(GP_GB^2 + (2*PI*F_GB*CP_GB)^2)*RS AR = G – (G2 + (2πfC)2)RS
CADJ	Corrected capacitance by compensating series resistance: CADJ = ((GP_GB^2) + (2*PI*F_GB*CP_GB)^2)*(CP_GB)/(AR^2 + (2*PI*F_GB*CP_GB)^2)
COX	Oxide capacitance (usually set to max capacitance in accumulation): COX = MAX(MAVG(CADJ, 2))+1E-15

Appendix B: References

1. Nicollian, E.H. and Brews, J.R. MOS Physics and Technology, Wiley, New York (1982)

2. Schroder, D.K. Semiconductor Material and Device Characterization, 2nd edition (New York, Wiley, 1998)

3. Keithley application notes:

   "C-V Characterization of MOS Capacitors Using the 4200A-SCS Parameter Analyzer".

   "Making Optimal Capacitance and AC Impedance Measurements with the 4200A-SCS Parameter Analyzer".

   "Performing Very Low Frequency Capacitance-Voltage Measurements on High Impedance Devices Using the 4200A-SCS Parameter Analyzer".

   "Switching Between C-V and I-V Measurements Using the 4200A-CVIV Multi-Switch and 4200A-SCS Parameter Analyzer".

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